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PATENT ABSTRACTS OF JAPAN

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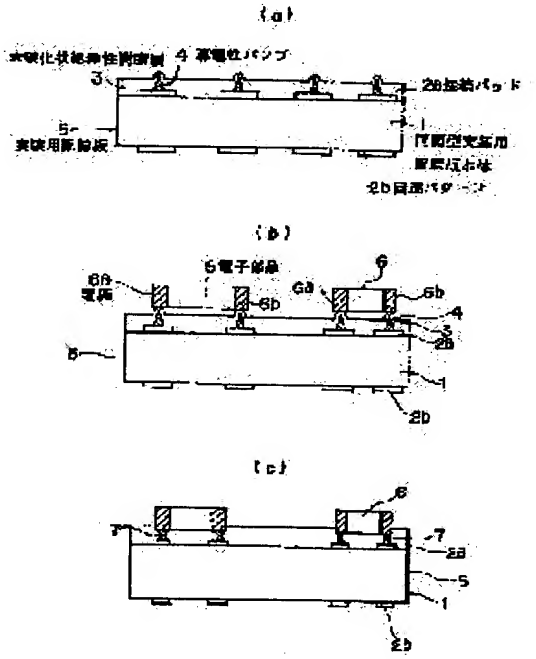
(71)Applicant : TOSHIBA CORP
(72)Inventor : OHIRA HIROSHI

(54) WIRING BOARD AND MOUNTING METHOD USING IT

(57)Abstract:

PURPOSE: To obtain a circuit device of high reliability at low cost by covering with an unhardened insulating resin layer at least part of a surface of a wiring board for mounting equipped with a group of conductive bumps, which has a connection pad group, each equipped with a conductive bump.

CONSTITUTION: A chip mounter is used for a conductive bump 4 of a wiring board 5 for mounting to match, position and arrange electrodes 6a and 6b of a chip-shape resistant element. For this positioning arrangement, a weight is applied instantaneously to the chip mounter to make the tip of the conductive bump 4 in a crushed shape, thus reducing the conductive bump 4 height. Next, this is left in room temperature to harden a room-temperature hardening type silicone resin as an unhardened-shape insulating resin layer 3. This enables the unhardened insulating resin layer 3 to isolate and insulate each connecting part. On the other hand, once it is hardened, its connecting parts are protected from the outer surface and making packaged electronic parts and the wiring board into one unit and fixing it are promoted, thus obtaining the packaged circuit device of high reliability.



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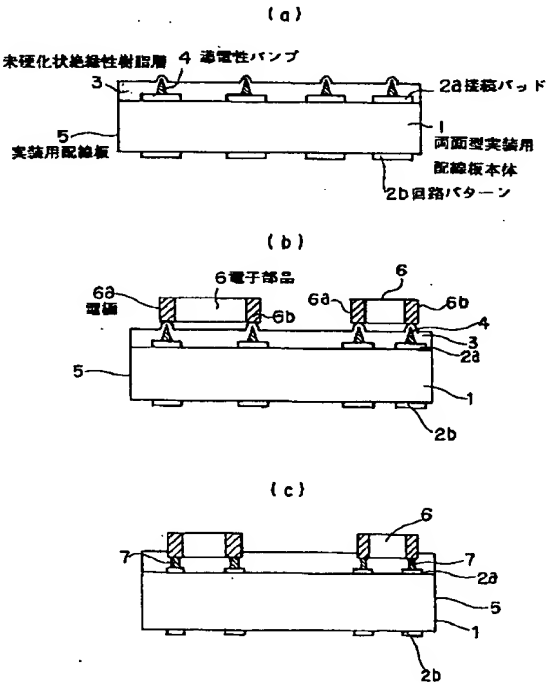
(54)【発明の名称】　実装用配線板およびこれを用いた実装方法

(57)【要約】

【目的】　低コストでありながら、信頼性の高い実装回路装置の構成に適する実装用配線板および実装方法の提供を目的とする。

【構成】　実装用配線板５は、搭載する電子部品６の電極6a，6b群に対応する接続パッド2a群を少なくとも一主面に有する実装用配線板５であって、前記実装用配線板５面の接続パッド2a群がそれぞれ導電性バンプ４を備え、かつ導電性バンプ４群を備えた面の少なくとも一部が未硬化状の絶縁樹脂層３で被覆されて成ることを特徴とし、実装方法は、少なくとも一主面に導電性バンプ４を備えた接続パッド2a群が形成され、かつ導電性バンプ４群を備えた面の少なくとも一部が未硬化状の絶縁樹脂層３で被覆されて成る配線板面上に、前記導電性バンプ４群に対応する電極6a，6b群を有する電子部品６を位置合わせして搭載・配置する工程と、前記位置合わせした配線板の導電性バンプ４群および電子部品６の電極6a，6b群の間にそれぞれ応力が作用するように電子部品を実装する工程と、前記配線板面の絶縁樹脂層３を硬化する工程とを具備して成ることを特徴とする。



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【特許請求の範囲】

【請求項１】　搭載する電子部品の電極群に対応する接続パッド群を少なくとも一主面に有する実装用配線板であって、

前記実装用配線板面の接続パッド群がそれぞれ導電性バンプを備え、かつ導電性バンプ群を備えた面の少なくとも一部が未硬化状の絶縁樹脂層で被覆されて成ることを特徴とする実装用配線板

【請求項２】少なくとも一主面に導電性バンプを備えた接続パッド群が形成され、かつ導電性バンプ群を備えた面の少なくともが未硬化状の絶縁樹脂層で被覆されて成る配線板面上に、前記導電性バンプ群に対応する電極群を有する電子部品を位置合わせして搭載・配置する工程と、

前記位置合わせした配線板の導電性バンプ群および電子部品の電極群の間にそれぞれ応力が作用するように電子部品を実装する工程と、

前記配線板面の絶縁樹脂層を硬化する工程とを具備して成ることを特徴とする実装方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は電子部品の面実装に適する実装用配線板およびこの実装用配線板を用いた実装方法に関する。

【０００２】

【従来の技術】電子機器類の軽小化ないしコンパクト化を目的として、回路機構の小形化なども図られている。すなわち、面実装用のパッドを有する配線板面に、所要の電子部品を実装して成る実装回路装置（実装回路ユニット）が、各種の電子機器類で広く実用に供されつつある。そして、前記電子部品の実装には、ハンダ付けによる実装方法が多用されている。具体的には、実装用配線板の導体ターンの所定位置、すなわち搭載する電子部品の電極に対応して設けられている各接続パッド面に、クリーム状にしたハンダペーストを印刷した後、電子部品の電極群を対応する接続パッド面に位置を合わせて搭載・配置し、リロフー炉を通過させてハンダーペーストを溶かし、冷却固化し、電子部品を配線板上に固定する方法が一般的に採用されている。なお、この工程においては、前記配線板面の各接続パッド、もしくは電子部品の電極面に金属バンプを設けておく場合もある。

【０００３】

【発明が解決しようとする課題】前記したように、配線板面への電子部品の実装は、ハンダ付け（ハンダ接続）法が一般的であるが、ハンダ付け法にはいろいろの問題点がある。具体的には、

(a)ハンダを溶融するために 200℃～ 300℃の温度が必要であり、したがって、実装用の配線板については、前記温度に耐える耐熱性が要求され、また、搭載する電子部品も、前記温度に耐え得るように耐熱保護を予め施しておくことを要する。こうした要求に対しては、比較的高価な材料を使う必要があり、また使用環境に対して、必要以上の耐熱保護が必要になるという問題がある。

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【０００４】(b)また、前記 200℃～ 300℃のハンダ溶融温度にて、ストレスフリーでハンダ付けされた電子部品は冷却過程で、電子部品と配線板の熱膨張率の差によって、常温時に大きなストレスを内蔵することになる。このため、各種環境での長期使用により、接続固定部、特に応力の集中するハンダ付け部が金属疲労を起こして、断線するといった不具合が生じる場合がある。

【０００５】(c)さらに、ハンダ付けにはフラックスが必要であり、クリームハンダの場合は、予めハンダペーストの中に配合してある。そして、このフラックスは、ハンダ溶融時に分解して酸性あるいはアルカリ性を呈して、配線板の導体パターン面（たとえば銅箔面），あるいは電子部品の電極の酸化物を除去して、ハンダ付けを助長する作用がある。しかし、一方では、フラックスの分解物が電気回路の絶縁性を低下させるという有害作用があるので、ハンダ付け後、洗浄処理などにより除去する必要がある。この除去には、一般的にフロンもしくは他の有機溶剤の使用を要し、その廃液の地球環境に対する悪影響から、代替策が求められている。　(d)高密度実装回路化に伴って、配線板の配線ピッチが微細になると、溶融ハンダが隣接する配線パターン同士がブリッジするという不具合も増大してきている。

【０００６】本発明は前記ハンダ付け実装における問題を解消（回避）し、低コストでありながら、信頼性の高い実装回路装置の構成に適する実装用配線板および実装方法の提供を目的とする。

【０００７】

【課題を解決するための手段】本発明に係る実装用配線板は、搭載する電子部品の電極群に対応する接続パッド群を少なくとも一主面に有する実装用配線板であって、前記実装用配線板面の接続パッド群がそれぞれ導電性バンプを備え、かつ導電性バンプ群を備えた面の少なくとも一部が未硬化状の絶縁樹脂層で被覆されて成ることを特徴とし、また、　本発明に係る実装方法は、少なくとも一主面に導電性バンプを備えた接続パッド群が形成され、かつ導電性バンプ群を備えた面の少なくとも一部が未硬化状の絶縁樹脂層で被覆されて成る配線板面上に、前記導電性バンプ群に対応する電極群を有する電子部品を位置合わせして搭載・配置する工程と、前記位置合わせした配線板の導電性バンプ群および電子部品の電極群の間にそれぞれ応力が作用するように電子部品を実装する工程と、前記配線板面の絶縁樹脂層を硬化する工程とを具備して成ることを特徴とする。

【０００８】そして、本発明は次のよう知見に基づいて成されたものである。つまり、通常の金属は、表面が酸化物ないし有機物で汚れており、導電性の液体、たとえば導電ペーストなどを接触もしくは塗布固着させても、

その界面にかなり大きな界面抵抗が存在する。しかも、その界面抵抗は、温度，湿度などの環境で容易に大きく変動し易く、電子回路には適用し得なかったが、適度の硬度を有した導電性バンプに、電子部品の電極を成す金属を押し当て、さらに応力を作用させると、金属表面の汚れが機械的に排除されて新生面を露出し、金属の新生面および導電バンプの新生面が、界面抵抗零の接合を容易に形成することを見出して、この現象を利用して本発明を完成するに至ったものである。

【０００９】本発明において、実装用配線板は、たとえばソルダーレジストを印刷し、仕上げ処理する前の、外層回路パターン上の所定位置に、導電性バンプ群を形成する一方、それら導電性バンプ群をほぼ埋める程度の厚さに、未硬化の絶縁性樹脂を一体的に設けることにより構成される。なお、未硬化の絶縁性樹脂層は、前記導電性バンプ群を形成した面全体に設ける必要はなく、たとえば各導電性バンプの周辺部など、島状に形成した形態を採ってもよい。

【００１０】ここで、印刷配線板の外層回路を形成する銅パターンなどは、各種の工程履歴において、表面が汚染されているので、機械研磨ないし化学研磨を行い清浄面にしてから、導電性バンプ群を形成することが望ましく、清浄面化しておくことにより、銅パターンと導電性バンプ群との界面抵抗の発生防止を助長し得る。また、前記導電性バンプは、たとえば銀，金，銅，ハンダ粉などの導電性粉末、これらの合金粉末もしくは複合の金属粉末と、たとえばポリカーボネート樹脂，ポリスルホン樹脂，ポリエステル樹脂，フェノキシ樹脂，エポキシ樹脂、フェノール樹脂，ポリイミド樹脂などのバインダー成分とを混合して調製された導電性組成物、あるいは導電性金属、導電性有機半導体などで構成される。そして、導電性組成物で形成する場合は、たとえば比較的厚いメタルマスクを用いた印刷法により、アスペクト比の高い導電性バンプを形成でき、その導電性バンプの高さは、一般的に10～ 400μｍ 程度の広範囲で形成できる。

【００１１】一方、導電性金属でバンプを形成する手段としては、 (a)銅箔を外層回路パターンとした場合は、メッキレジストを印刷・パターニングして、銅，錫，金，銀，ハンダなどをメッキして、選択的に微小な金属柱（バンプ）群の形成するか、(b)外層回路パターン面にハンダレジストの塗布・パターニングを行ってから、ハンダ浴に浸漬して選択的に微小な金属柱（バンプ）の形成などが挙げられる。ここで、導電性バンプに相当する微小金属塊ないし微小な金属柱は、異種金属を組合わせて成る多層構造、多層シェル構造でもよい。

【００１２】なお、本発明において、導電性バンプを導電性組成物で形成する場合は、メッキ法などの手段で行う場合に較べて、さらに工程など簡略化し得るので、低コスト化の点で有効である。また、適度の硬度を有する導電性バンプとは、搭載・実装する電子部品の電極を成す金属面の酸化物や有機物などの汚染物層を、押圧力などによって対接面から機械的に排除し、金属の新生面を露出できる程度以上の応力を作用させた場合、電子部品の電極を変形ないし破壊しない程度の硬度を要し、一般的にはジュロメータ硬度で70～ 120が好適である。

【００１３】また、前記導電性バンプの大きさは、搭載・実装する電子部品の電極の大きさに対応させるが、上記導電性バンプの形成手段によって、径10～ 400μｍ 程度で任意に形成できる。またバンプの形状は底面が大きく先端部向かって細くなる形状が好適であり、山形ないし半球状などでもよい。

【００１４】前記導電性バンプを埋める程度の厚さに配線板面上に、一体的に配置形成されている未硬化状の絶縁樹脂層は、前記配線板の全面に配置形成してもよいし、必要部分にのみ、選択的に配置形成してもよいし、また、電子部品を搭載する直前に未硬化状の絶縁樹脂層を塗布形成する形態を採ってもよい。この絶縁樹脂層は、搭載された電子部品を固着する役割と、配線板の回路部を保護する役割と、接続部を保護する役割とを兼ね備える。そして、この絶縁樹脂層は、熱硬化型樹脂や紫外線硬化型樹脂、嫌気性硬化樹脂、もしくはそれらの混合タイプなどで形成しておき、電子部品搭載後紫外線ないし加熱で硬化させるのが好ましく、たとえばソルダーレジストとして市販されている樹脂が好適である。

【００１５】さらに、本発明の実装方法において、電子部品の電極と配線板の導電性バンプとを、応力の作用によって界面抵抗がほぼ零の接続を形成して実装する際、前記応力の付与は、通常、 0.5～20 N／バンプ当たり程度の力、導電性バンプの形状や材質によっては、未硬化状樹脂の硬化収縮性などでもよい。つまり、搭載・実装する電子部品は、通常、異なるメーカー製品の寄せ集めであるため、その保存期間も一定でなく、電極材料の種類も違うので、表面の汚れをなす酸化物層や有機物の種類、また、その厚さなども多様であるが、一般的に通常の電子部品では、汚染層の厚みがサブミクロンオーダーである。そして、この程度の厚みの汚染層は、前記適度の硬度を有した先端部の尖った導電性バンプを押し当てると、導電性バンプの突き当たり面で汚染層を排除できる。この具体的な手段としては、個々の電子部品の搭載時にもしくは全電子部品を搭載後に治具板など用いて一括して、電極部の上から力を作用させることにより行われる。

【００１６】なお、本発明において、実装する電子部品としては、セラミック材料から構成されるチップ型抵抗体、コンデンサー、或いはフラットリード、ガルリング型リード、Ｊリードなど各種の形状のリードあるＩＣパッケージ、コネクターなどの電子部品、また高密度実装のために、希に使用されるベアＩＣチップなどもが挙げられる。また、これら電子部品の電極は、貴金属製であってよいし、一般的な材料である錫鉛系ハンダ材料、錫

メッキ仕上げ、ニッケルメッキ仕上げ、銅、アルミニューム薄膜などの材質で形成されていてもよい。

【００１７】

【作用】上記本発明に係る実装用配線板においては、搭載・実装する電子部品の電極に対応した導電性バンプが未硬化な絶縁樹脂層に埋め込まれた形に設置されており、また、前記導電性バンプは応力の作用によって薄い酸化物層などを破壊して新しい金属面を露出させる機能を呈する。したがって、位置合わせ後、応力を作用させることにより、前記導電性バンプに対して、搭載・実装する電子部品の電極を界面抵抗零の状態で電気的な接続を達成する。しかも、前記未硬化な絶縁樹脂層が各接続部を互いに絶縁離隔する一方、硬化するとその接続部などを外界から保護するとともに、実装電子部品と配線板との一体・固定化を助長するので、信頼性の高い実装回路装置を提供し得ることになる。

【００１８】

【実施例】以下図１ (a)，(b)，(c)、図２ (a)，(b)，(c)、および図３ (a)，(b)，(c)を参照して本発明の実施例を説明する。

【００１９】実施例１

図１ (a)は、本発明に係る実装用配線板例を断面的に、また図１ (b)は図１ (a)に図示した実装用配線板に電子部品を実装する態様を模式的に示す断面図、図１ (c)は図１ (b)に図示した実装する態様で応力を作用させて電子部品を実装した後の状態を模式的に示す断面図である。

【００２０】先ず、図１ (a)において、１は両面型実装用配線板本体、2aは前記両面型実装用配線板本体１の接続パッドを成す銅パターン、2bは回路パターン、３は前記接続パッド２形成面に一体的に積層配置された未硬化状の絶縁性樹脂層、４は前記接続パッド２面に形成配置された導電性バンプである。さらに具体的には、両面型実装用配線板本体１は、ガラスクロス入りエポキシ樹脂を基材とし、接続パッド2a，回路パターン2bの厚さが35μｍ、接続パッド2aの形状が 0.9× 1.2㎜、導電性バンプ４が高さ60μｍ の山形、未硬化状の絶縁性樹脂層３が厚さ40μｍ の室温硬化型シリコーン樹脂層で、1608タイプの抵抗素子を搭載・実装可能な、全体の厚さが 1.0㎜の実装用配線板５である。

【００２１】そして、前記構成の実装用配線板５は、次のようにして製造し得る。すなわち、一般的な手段で製造した両面型実装用配線板本体１を先ず用意し、接続パッド2a形成面を回転式ブラシで研磨してから、水洗後空冷乾燥した。次いで、手早く、板厚 300μｍ のアルミ板の所定箇所に 0.3㎜径の穴を明けたメタルマスクを用いて、前記両面型実装用配線板本体１の接続パッド2a面上に、前記メタルマスクの穴を位置決め配置して、ポリマータイプの銀系の導電性ペーストを印刷し、高さ約60μｍ の山形の導電性バンプ４を形成（形設）した。その後、 120℃で30分間加熱硬化し、粘着絶縁樹脂層（未硬化状の絶縁樹脂層）３として室温硬化型シリコーン樹脂（信越化学ＫＫ製，商品名， RTVゴム，KF3498）を40μｍ 厚さで塗布することにより製造した。

【００２２】前記構成の実装用配線板５に対する電子部品６の実装、たとえばチップ形の抵抗素子の実装は、次のように行われる。すなわち、前記実装用配線板５の導電性バンプ４に、チップマウンターを用いて、図１ (b)に示すごとく、前記チップ形の抵抗素子６の電極6a，6bを対応させて位置決め配置する。この位置決め配置に当たって、チップマウンターに瞬間的に 5.0 Nの加重を加えたところ、図１ (c)に示したように、前記導電性バンプ４の先端部が潰れた形になり、導電性バンプ４の高さは30μｍ に減じた。次いで、これを24時間室温下に放置して、シリコーン樹脂３を硬化させた。

【００２３】上記実装した実装回路において、チップ形の抵抗素子６は抵抗素子として、電気的に十分な機能を有し、熱衝撃試験（−65℃～ 125℃，1000ｈ）、加熱試験（ 125℃，1000ｈ）、耐湿試験（80℃，85％総耐湿度，1000ｈ）など加速信頼性試験にも問題はなかった。

【００２４】実施例２

図２ (a)は、本発明に係る他の実装用配線板例を断面的に、また図２ (b)は図２ (a)に図示した実装用配線板に電子部品を実装する態様を模式的に示す断面図、図２ (c)は図２ (b)に図示した実装する態様で応力を作用させて電子部品を実装した後の状態を模式的に示す断面図である。

【００２５】実施例１の場合に準じて、図２ (a)に断面的に示すような、28ピンのリードを有するガルリングタイプのFPパッケージタイプのＩＣメモリ６を実装し得る導電性バンプ４を備えた構成の実装用配線板５を用意した。なお、前記実装用配線板５の接続パッド2aの形状は、 0.8× 1.6㎜角で、最小1.25㎜ピッチであり、また導電性バンプ４は高さ約50μｍ の山形を成していた。そして、前記実装用配線板５面に、ＩＣメモリ６のリード6aを対応する導電性バンプ４と位置合わせ・配置し、図２ (b)に断面的に示すごとく、リード6a，6bの平坦面に20 Nの力を作用させ、導電性バンプ４の高さが約35μｍ 程度になるよう押圧して実装を行った。

【００２６】こうして構成した図２ (c)に断面的に示すような、ＩＣメモリー実装回路装置は、電気的に十分な機能を呈し、熱衝撃試験（−65℃～ 125℃，1000ｈ）、加熱試験（ 125℃，1000ｈ）、耐湿試験（80℃，85％総耐湿度，1000ｈ）など加速信頼性試験にも問題はなかった。

【００２７】実施例３

先ず、基材がガラスクロス入りエポキシ樹脂からなる常法により製造した厚みは 1.0㎜で銅パターンの厚みは18μｍ で、 100μｍ 角，最小ピッチ 150μｍ，表面を薄いニッケル、金メッキで被覆した接続パッド2a群を備え

た、図３ (a)に断面的に示すような配線板を素材とし、実施例１の場合に準じてメタルマスクを介して高さ約30μm の山形状の導電性バンプ４を設け、かつその導電性バンプ４形設置面に、未硬化状の絶縁性樹脂層３を設けて成る実装用配線板５を用意した。一方、 100μm 角で，約 1μm 厚，最小ピッチ 150μm のアルミニューム薄膜製I/O端子を有するＩＣメモリーチップ（チップ寸法，15×10㎜角）を電子部品として用意した。ここで、実装用配線板５の導電性バンプ４は、平均粒径 0.5μm の鱗片状銀粉とビスフェノールタイプのエポキシ樹脂とから成る導電性ペーストを印刷し、 120℃で30分間加熱硬化処理して形成し、また未硬化状の絶縁性樹脂層３は、ソルダーレジスト（商品名．UVR-150R，太陽インキKK）を約30μm の厚さに塗布して形成した。

【００２８】前記実装用配線板５面にＩＣメモリーチップ６を、図３ (b)に断面的に示すごとく、相互の導電性バンプ４および I/O端子6a，6bを位置合わせして搭載・配置した後、ＩＣメモリーチップ６の上から均一に加重がかかるように、20 Nの加重をかけたところ、前記導電性バンプ４の高さが15μm に減じ、これを紫外線照射炉に収容し、未硬化状の絶縁性樹脂層３を硬化させ、さらに 120℃で30分間加熱して完全硬化させて、図３ (c)に断面的に示すような、実装回路装置を構成した。　上記、構成した実装回路装置は、電気的に十分な機能を有し、熱衝撃試験（－65℃～ 125℃，1000ｈ）、加熱試験（ 125℃，1000ｈ）、耐湿試験（80℃，85％総耐湿度，1000ｈ）など加速信頼性試験にも問題はなかった。

【００２９】

【発明の効果】本発明に係る実装用配線板によれば、従来電子部品の実装において提起しているハンダ接続による問題を容易に回避し得る。具体的には、 (1)常温ないし 100℃程度のプロセス温度で電子部品の実装・接続が可能となり、高級な耐熱材料を配線板や電子部品にも使わなくてもよくなる。 (2)前記のように低温での接続が可能であるため、配線板と電子部品との熱膨張率の差によるストレスも小さく押さえられ、接続部の剥離などの発生が抑制されて長期使用に耐えるようになる。(3)ハンダ接続に使用するフラックスなど電気的に有害物を使用しないですむので、環境上の問題も発生しない。 (4)配線のピッチが微細になっても、導電性バンプを微細に形成することにより、電子部品との確実な電気的な接合が図られ、かつ隣接する接続部同士のパターンがブリッジするという不具合も生じない。かくして、本発明に係る実装用配線板、およびこの実装用配線板を用いる実装方法は、実用上多くの利点をもたらすものといえる。

【図面の簡単な説明】

【図１】本発明に係る実装用配線板および実装方法を例示するもので、 (a)は実装用配線板の断面図、 (b)はチップ形電子部品の搭載した状態を模式的に示すの断面図、(C) 電子部品を実装して形成した実装回路装置の断面図。

【図２】本発明に係る実装用配線板および実装方法の他の例を示すもので、 (a)は実装用配線板の断面図、 (b)はリード付きＩＣの搭載した状態を模式的に示すの断面図、(C) 電子部品を実装して形成した実装回路装置の断面図。

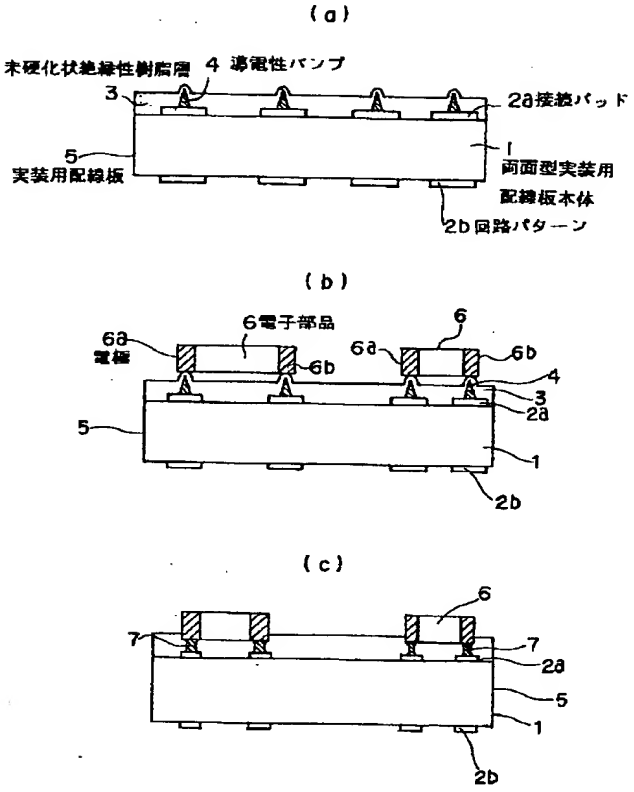
【図３】本発明に係る実装用配線板および実装方法のさらに他の例を示すもので、 (a)は実装用配線板の断面図、 (b)はベアのチップＩＣの搭載した状態を模式的に示すの断面図、(C) 電子部品を実装して形成した実装回路装置の断面図。

【符号の説明】

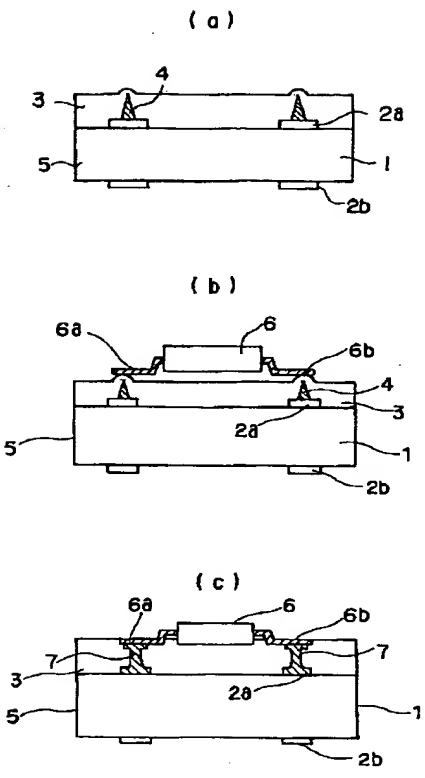
１…両面型実装用配線板本体　　2a…接続パッド　　2b…回路パターン

３…未硬化の絶縁性樹脂層　　４…導電性バンプ　　５…実装用配線板　　６…搭載・実装電子部品　　6a，6b…電極（端子）　　７…潰れた導電性バンプ

【図１】

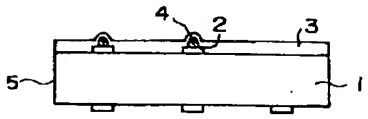

(a)
未硬化状絶縁性樹脂層
4 導電性バンプ
3
2a接続パッド
5
実装用配線板
1
両面型実装用
配線板本体
2b回路パターン
(b)
6電子部品
6a
電極
6
6a
6b
6b
4
3
2a
5
1
2b
(c)
6
7
7
2a
5
1
2b

【図２】

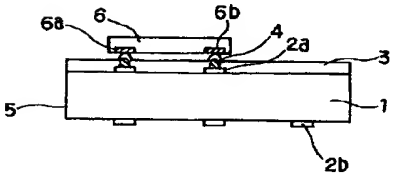

(a)
4
3
2a
5
1
2b
(b)
6a
6
6b
4
3
2a
5
1
2b
(c)
6a
6
6b
7
7
3
2a
5
1
2b

【図３】

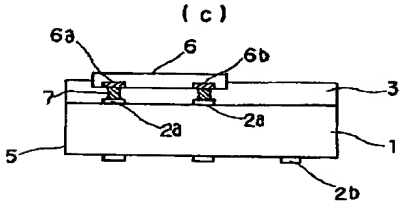
(a)



(b)



(c)



* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention relates to the mounting method using the real wearing patchboard suitable for the surface mounting of electronic parts, and this real wearing patchboard.
[0002]
[Description of the Prior Art] The miniaturization of a circuit mechanism etc. is attained for the purpose of ****-izing or miniaturization of electronic equipment. That is, practical use is being widely presented with the mounting circuit apparatus (mounting circuit unit) which mounts necessary electronic parts in the patchboard side which has a pad for surface mounting, and grows into it by various kinds of electronic equipment. And the mounting method by soldering is used abundantly at mounting of the aforementioned electronic parts. concrete -- the conductor of a real wearing patchboard -- to each connection pad side established corresponding to the electrode of the electronic parts which, namely, a turn carries [predetermined] After printing the creamed pewter paste, a position is doubled with the connection pad side which corresponds the electrode group of electronic parts, it arranges, and a RIROFU furnace is passed, a HANDA paste is melted, cooling solidification is carried out, and, generally loading and the method of fixing electronic parts on a patchboard are adopted. In addition, in this process, the metal bump may be prepared in the electrode side of each connection pad of the aforementioned patchboard side, or electronic parts.
[0003]
[Problem(s) to be Solved by the Invention] Although mounting of the electronic parts to a patchboard side has the common soldering (pewter connection) method as described above, there are various troubles in the soldering method. In order to specifically fuse the (a) pewter The temperature of 200 degrees C - 300 degree C is required, therefore it requires giving heat-resistant protection beforehand so that the electronic parts which the thermal resistance which bears the aforementioned temperature is required, and are carried about the patchboard of real wearing can also be borne at the aforementioned temperature. It is necessary to use a comparatively expensive material and, and there is a problem that the heat-resistant protection more than required is needed, to an operating environment to such a demand.
[0004] (b) Moreover, the above The electronic parts soldered by the stress free-lancer with the pewter melting temperature of 200 degrees C - 300 degree C are cooling processes, and will contain a big stress according to the difference of the coefficient of thermal expansion of electronic parts and a patchboard at the time of ordinary temperature. For this reason, the fault that a connection fixed part, especially the soldering section which stress concentrates cause and disconnect the metal fatigue by long-term use in various environment may arise.
[0005] (c) Flux is still more nearly required for soldering, and when it is a cream pewter, it has blended into the pewter paste beforehand. And it decomposes at the time of pewter melting, and this flux presents acidity or alkalinity, removes the oxide of the conductor pattern side (for example, copper-foil face) of a patchboard, or the electrode of electronic parts, and has the operation which promotes

soldering. However, on the other hand, since there is detrimental operation that the decomposition product of flux reduces the insulation of an electrical circuit, washing processing etc. needs to remove after soldering. Generally this removal takes use of chlorofluocarbon or other organic solvents, and the alternative plan is demanded from it from the bad influence to the earth environment of the waste fluid. (d) If the wiring pitch of a patchboard becomes detailed with the formation of a high-density-assembly circuit, the fault that the circuit patterns which a melting pewter adjoins carry out a bridge will also increase.

[0006] this invention solves the problem in the aforementioned soldering mounting (evasion), and though it is a low cost, it aims at offer of the real wearing patchboard suitable for the composition of a reliable mounting circuit apparatus, and the mounting method.

[0007]

[Means for Solving the Problem] The real wearing patchboard concerning this invention is a real wearing patchboard which has a connection pad group corresponding to the electrode group of the electronic parts to carry in at least 1 principal plane. The connection pad group of the aforementioned patchboard side for mounting is equipped with a conductive bump, respectively. and the thing which a part of field [at least] equipped with the conductive bump group is covered with an un-hardening-like insulating resin layer, and it changes -- the feature -- carrying out -- moreover -- The mounting method concerning this invention The connection pad group which equipped at least 1 principal plane with the conductive bump is formed. Alignment of the electronic parts which have an electrode group corresponding to the aforementioned conductive bump group on the patchboard side where a part of field [at least] equipped with the conductive bump group is covered with an un-hardening-like insulating resin layer, and it changes is carried out. And loading and the process to arrange, It is characterized by providing the process which mounts electronic parts so that stress may act, respectively between the conductive bump group of the patchboard which carried out [aforementioned] alignment, and the electrode group of electronic parts, and the process which hardens the insulating resin layer of the aforementioned patchboard side, and changing.

[0008] And this invention is accomplished based on as-follows knowledge. That is, even if the front face is dirty with an oxide or the organic substance and, as for the usual metal, contacts or fixes [application] a conductive liquid, for example, conductive paste etc., a quite big interfacial resistance exists in the interface. And although it tends to change the interfacial resistance sharply easily in environments, such as temperature and humidity, and could not apply to an electronic circuitry If the metal which accomplishes the electrode of electronic parts is pressed against a conductive bump with the moderate degree of hardness and stress is made to act further The dirt of a surface of metal is eliminated mechanically, a new field is exposed, a metaled new field and an electric conduction bump's new field find out forming junction of interfacial-resistance zero easily, and it comes to complete this invention using this phenomenon.

[0009] In this invention, a real wearing patchboard is constituted by preparing an insulating non-hardened resin in the thickness of the grade which buries these conductivity bump group mostly in one, while forming a conductive bump group in the predetermined position on an outer layer circuit pattern before printing, finishing and processing a solder resist. In addition, an insulating non-hardened resin layer may take the gestalt which did not need to prepare in the whole field in which the aforementioned conductive bump group was formed, for example, was formed in the shape of [, such as each conductive bump's periphery,] an island.

[0010] Here, in various kinds of process histories, since the front face is polluted, after the copper pattern which forms the outer layer circuit of a printed circuit board performs mechanical polishing or chemical polishing and makes it a pure side, it is desirable to form a conductive bump group and it can promote generating prevention of the interfacial resistance of a copper pattern and a conductive bump group by forming the pure side. Moreover, the aforementioned conductive bump consists of a conductive constituent which mixed a metal powder conductive powder, such as silver, gold, copper, and pewter powder, these end of an alloy powder, or compound, and binder components, such as polycarbonate resin, polysulfone resin, polyester resin, a phenoxy resin, an epoxy resin, phenol resin,

and polyimide resin, and was prepared or a conductive metal, a conductive organic semiconductor, etc. And when forming with a conductive constituent, the conductive high bump of an aspect ratio can be formed by the print processes using the comparatively thick metal mask, and generally the conductive bump's height is ten to 400 micrometer. It can form by the large area of a grade.
[0011] On the other hand as a means to form a bump with a conductive metal When (a) copper foil is used as an outer layer circuit pattern Carry out a plating resist printing and patterning, and copper, tin, gold, silver, a pewter, etc. are plated. alternative -- a minute metal pillar (bump) group -- forming -- or -- (b) outer layer circuit pattern side -- a pewter resist -- after performing application and patterning, it is immersed in a pewter bath and formation of a minute metal pillar (bump) etc. is mentioned alternatively Here, the multilayer structure and the multilayer shell structure which change combining a dissimilar metal are sufficient as the minute metal soul or the minute metal pillar equivalent to a conductive bump.
[0012] In addition, in this invention, since it can process-etc.-simplify further compared with the case where it carries out with meanses, such as plating, when forming a conductive bump with a conductive constituent, it is effective in respect of low-cost-izing. Moreover, contamination layers which accomplish the electrode of the electronic parts carried and mounted, such as an oxide of a metal side and the organic substance, are mechanically eliminated from an opposite plane of composition according to the press force etc., the degree of hardness of the grade which does not deform or destroy the electrode of electronic parts when the stress beyond the grade which can expose a metaled new field is made to act is required, and, generally 70-120 are suitable for the conductive bump who has a moderate degree of hardness by the durometer degree of hardness.
[0013] Moreover, the aforementioned conductive bump's size is a ten to 400 micrometer diameter by the above-mentioned conductive bump's means forming, although it is made to correspond to the size of the electrode of the electronic parts carried and mounted. It can form arbitrarily by the grade. Moreover, the configuration to which is a base ******** greatly and becomes thin may be suitable for a bump's configuration, and the shape of Yamagata or a semi-sphere etc. has as it.
[0014] The insulating resin layer of the shape of un-hardening [by which arrangement formation is carried out in one on the patchboard side at the thickness of the grade which buries the aforementioned conductive bump] may carry out arrangement formation all over the aforementioned patchboard, and you may take the gestalt carry out application formation in an un-hardening-like insulating resin layer just before carrying out arrangement formation alternatively and carrying electronic parts only to a required portion. This insulating resin layer combines the role which fixes the carried electronic parts, the role from which the circuit section of a patchboard is protected, and the role from which a connection is protected. And as for this insulating resin layer, it is desirable to form by the heat-hardened type resin, the ultraviolet-rays hardening type resin, anaerobic hardening resin, or those mixed types, and to make it harden by after [electronic-parts loading] ultraviolet rays or heating, for example, the resin marketed as a solder resist is suitable for it.
[0015] Furthermore, in case an interfacial resistance forms connection of about zero and mounts the electrode of electronic parts, and the conductive bump of a patchboard by operation of stress, depending on configuration and the quality of the material of the force about per 0.5 - 20 N / bump, and a conductive bump, the hardening shrinkage characteristics of an un-hardening-like resin etc. are usually sufficient as grant of the aforementioned stress in the mounting method of this invention. That is, although the kind of the oxide layer and the organic substance with which the electronic parts carried and mounted form surface dirt since the retention period is not fixed, either, since it is usually the medley of a different maker product, and the kind of electrode material is also different, its thickness, etc. are various, generally in the usual electronic parts, the thickness of a pollution layer is submicron order. and the pollution layer of thickness of this level -- the above -- if the conductive bump by whom the point with the moderate degree of hardness sharpened is pressed, a pollution layer can be eliminated in respect of the end of a conductive bump the time of loading of each electronic parts as this concrete means -- or after carrying all electronic parts, a fixture board etc. is used and put in block, and it is carried out by making the upper shell force of the polar zone act
[0016] in addition, the Lead of various kinds of configurations, such as a tipped type resistor which

consists of ceramic material in this invention as electronic parts to mount, a capacitor or a flat lead, the Galle ring-type lead, and J lead, -- the raise in basic wages IC chip rarely used for electronic parts, such as a certain IC package and a connector, and high density assembly -- although -- it is mentioned Moreover, the electrode of these electronic parts may be formed with the quality of the materials, such as **** system pewter material which may be a product made from noble metals and is a general material, tinning finishing, nickel-plating finishing, copper, and an aluminum thin film.
[0017]
[Function] In the real wearing patchboard concerning the above-mentioned this invention, it is installed in the form where loading and the conductive bump corresponding to the electrode of electronic parts to mount were embedded in the insulating resin layer [**** / un-], and the aforementioned conductive bump presents the function to which a thin oxide layer etc. is destroyed and a new metal side is exposed by operation of stress. Therefore, electric connection is attained for loading and the electrode of electronic parts to mount in the state of interfacial-resistance zero to the aforementioned conductive bump by making stress act after alignment. and the above -- since - fixation is really [of mounting electronic parts and a patchboard] promoted while an insulating resin layer [**** / un-] carries out insulating isolation of each connection mutually and protecting the connection etc. from the external world if it hardens, a reliable mounting circuit apparatus can be offered
[0018]
[Example] Following drawing 1 (a), (b), (c), drawing 2 (a), (b), (c) and drawing 3 (a), The example of this invention is explained with reference to (b) and (c).
[0019] Example 1 drawing 1 (a) is drawing 1 in cross section about the example of a real wearing patchboard concerning this invention again. (b) is drawing 1 . The cross section, drawing 1 which show the mode which mounts electronic parts typically to the real wearing patchboard illustrated to (a) (c) is drawing 1 . It is the cross section showing typically the state after making stress act in the mode which was illustrated to (b), and to mount and mounting electronic parts.
[0020] First, drawing 1 In (a), the copper pattern with which the main part of a both-sides type real wearing patchboard and 2a accomplish the connection pad of the aforementioned main part 1 of a both-sides type real wearing patchboard in 1, the insulating resin layer of the shape of un-hardening [by which laminating arrangement of the 2b was carried out in / a circuit pattern and 3 / the connection pad 2 aforementioned forming face / one], and 4 are the conductive bumps by whom formation arrangement was done at the 2nd page of the Still more specifically the main part 1 of a both-sides type real wearing patchboard the epoxy resin containing glass fabrics -- a base material -- carrying out -- the thickness of connection pad 2a and circuit pattern 2b -- 35 micrometers The configuration of connection pad 2a 0.9x1.2 mm and the conductive bump 4 are a height of 60 micrometers. The insulating resin layer 3 of the shape of Yamagata and un-hardening is 40 micrometers in thickness. In a room-temperature-curing type silicone resin layer The whole thickness which can mount [loading and] the resistance element of 1608 types It is the real wearing patchboard 5 which is 1.0mm.
[0021] And the real wearing patchboard 5 of the aforementioned composition can be manufactured as follows. That is, after preparing first the main part 1 of a both-sides type real wearing patchboard manufactured with the general means and grinding the connection pad 2a forming face with the rotating type brush, after [rinsing] air-cooling dryness was carried out. Subsequently, it is quick and is board thickness. 300 micrometers In the predetermined part of an aluminum board Using the metal mask which ended the hole of the diameter of 0.3mm, positioning arrangement of the hole of the aforementioned metal mask is carried out, the conductive paste of a polymer type silver system is printed on connection pad 2 the a-th page of the aforementioned main part 1 of a both-sides type real wearing patchboard, and it is a height of about 60 micrometers. Conductive PAMBU 4 of Yamagata was formed (assemblage) Then, heat hardening is carried out for 30 minutes at 120 degree C, and it is 40 micrometers about room-temperature-curing type silicone resin (the product made from Shin-etsu chemistry KK, a tradename, RTV rubber, KF3498) as an adhesion insulation resin layer (un-hardening-like insulating resin layer) 3. It manufactured by applying by thickness.
[0022] Mounting of electronic parts 6 to the real wearing patchboard 5 of the aforementioned

composition, for example, mounting of a tipped type resistance element, is performed as follows. That is, a chip mounter is used for conductive PAMBU 4 of the aforementioned patchboard 5 for mounting, and it is drawing 1 . The electrodes 6a and 6b of the resistance element 6 of the aforementioned chip type are made to correspond to (b) so that it may be shown, and positioning arrangement is carried out. It is in charge of this positioning arrangement, and is to a chip mounter. It is drawing 1 when the load of 5.0 N was added. Becoming the form where the aforementioned conductive bump's 4 point was crushed as shown in (c), the conductive bump's 4 height is 30 micrometers. It reduced. Subsequently, this was left under the 24-hour room temperature, and silicone resin 3 was stiffened.

[0023] In the mounting circuit which carried out [above-mentioned] mounting, as a resistance element, the tipped type resistance element 6 has sufficient function electrically, and the problem did not have it in acceleration reliability trials, such as a spalling test (-65 degrees C - 125 degree C, 1000h), a heat test (125 degree C, 1000h), and a humidity resistance test (80 degrees C, the moisture-proof 85% total degree, 1000h),, either.

[0024] Example 2 drawing 2 (a) is drawing 2 in cross section about other examples of a real wearing patchboard concerning this invention again. (b) is drawing 2 . The cross section, drawing 2 which show the mode which mounts electronic parts typically to the real wearing patchboard illustrated to (a) (c) is drawing 2 . It is the cross section showing typically the state after making stress act in the mode which was illustrated to (b), and to mount and mounting electronic parts.

[0025] In the case of an example 1, it applies correspondingly, and is drawing 2 . The real wearing patchboard 5 of composition of having had conductive PAMBU 4 which can mount IC memory 6 gal ring type FP package type which has the lead of 28 pins as shown in (a) in cross section was prepared. In addition, it is the configuration of connection pad 2a of the aforementioned patchboard 5 for mounting, and a 0.8x 1.6mm angle, and is a minimum of 1.25mm pitch, and the conductive bump 4 is a height of about 50 micrometers. Yamagata was accomplished. And alignment and arrangement of lead 6a of IC memory 6 are done with conductive PAMBU 4 corresponding to the 5th page of the aforementioned patchboard for mounting, and it is drawing 2 . The force of 20 N is made to act on the flat side of Leads 6a and 6b, as shown in (b) in cross section, and the height of conductive PAMBU 4 is about 35 micrometers. It mounted by pressing so that it may become a grade.

[0026] In this way, constituted drawing 2 The IC memory mounting circuit apparatus as shown in (c) in cross section presented sufficient function electrically, and it was satisfactory also to acceleration reliability trials, such as a spalling test (-65 degrees C - 125 degree C, 1000h), a heat test (125 degree C, 1000h), and a humidity resistance test (80 degrees C, the moisture-proof 85% total degree, 1000h).

[0027] an example 3 -- thickness first manufactured by the conventional method which a base material becomes from the epoxy resin containing glass fabrics 1.0mm -- the thickness of a copper pattern -- 18 micrometers it is -- 100 micrometers An angle, the minimum pitch 150 micrometers A front face Thin nickel, Drawing 3 equipped with the connection pad 2a group covered with gold plate Are made from a patchboard as shown in (a) in cross section. A metal mask is minded according to the case of an example 1, and it is a height of about 30 micrometers. The real wearing patchboard 5 which forms conductive BAMBU 4 of a mountain configuration, and forms the insulating un-hardening-like resin layer 3 in the conductive BAMBU 4 type installation side, and changes was prepared. On the other hand, it is 100 micrometer. At an angle, it is abbreviation. 1 micrometer **, the minimum pitch 150 micrometers IC memory chip (a chip size, 15x10mm angle) which has an I/O terminal made from an aluminum thin film was prepared as electronic parts. here -- the conductive bump 4 of the real wearing patchboard 5 -- mean particle diameter the conductive paste which consists of 0.5-micrometer scale-like silver dust and a bisphenol type epoxy resin is printed -- 120 degree C -- the heat-hardening processing during 30 minutes -- carrying out -- forming -- moreover, the insulating un-hardening-like resin layer 3 -- a solder resist (tradename .UVR-150R, solar ink KK) -- about 30 micrometers It applied to thickness and formed.

[0028] About the IC memory chip 6, it is drawing 3 in the 5th page of the aforementioned patchboard for mounting. As shown in (b) in cross section Mutual reaches conductive bump 4. So that alignment of the I/O terminals 6a and 6b is carried out, and a load may be applied to the upper shell homogeneity of the IC memory chip 6, after arranging, loading When the load of 20 N was applied, the aforementioned

conductive bump's 4 height is 15 micrometers. It reduces. This is held in a UV irradiation furnace, the insulating un-hardening-like resin layer 3 is stiffened, and it is a pan. At 120 degrees C, it heats for 30 minutes, full hardening is carried out, and it is drawing 3 . The mounting circuit apparatus as shown in (c) in cross section was constituted. The mounting circuit apparatus described above and constituted has sufficient function electrically, and it was satisfactory also to acceleration reliability trials, such as a spalling test (-65 degrees C - 125 degree C, 1000h), a heat test (125 degree C, 1000h), and a humidity resistance test (80 degrees C, the moisture-proof 85% total degree, 1000h).

[0029]

[Effect of the Invention] According to the real wearing patchboard concerning this invention, the problem by the pewter connection conventionally raised in mounting of electronic parts can be avoided easily. It is concrete. ** [there is no (1) ordinary temperature] Mounting and connection of electronic parts do not need to be attained at the process temperature of about 100 degrees C, and it becomes unnecessary to use a high-class heat-resisting material also for a patchboard or electronic parts. (2) Since connection at low temperature is possible as mentioned above, it is pressed down small, generating of ablation of a connection etc. is suppressed, and it also comes to bear the stress by the difference of the coefficient of thermal expansion of a patchboard and electronic parts at long-term use. (3) Since it is not necessary to use a detrimental object electrically, the problem on environment does not generate the flux used for pewter connection, either. (4) Even if the pitch of wiring becomes detailed, don't produce the fault that the pattern of the connections which positive electric junction to electronic parts is achieved, and adjoin carries out a bridge, by forming a conductive bump minutely, either. In this way, the mounting method using the real wearing patchboard concerning this invention and this real wearing patchboard can be called what brings about many advantages practically.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
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CLAIMS

[Claim(s)]
[Claim 1] The real wearing patchboard characterized by covering a part of field [at least] which it is the real wearing patchboard which has a connection pad group corresponding to the electrode group of the electronic parts to carry in at least 1 principal plane, and the connection pad group of the aforementioned patchboard side for mounting was equipped with the conductive bump, respectively, and was equipped with the conductive bump group with an un-hardening-like insulating resin layer, and changing [Claim 2] The mounting method characterized by providing the following even if there are few fields which the connection pad group which equipped at least 1 principal plane with the conductive bump was formed, and were equipped with the conductive bump group -- although -- the process which carries out alignment of the electronic parts which have an electrode group corresponding to the aforementioned conductive bump group, and does loading and arrangement of them on the patchboard side which is covered with an un-hardening-like insulating resin layer, and changes The process which mounts electronic parts so that stress may act, respectively between the conductive bump group of the patchboard which carried out [aforementioned] alignment, and the electrode group of electronic parts The process which hardens the insulating resin layer of the aforementioned patchboard side

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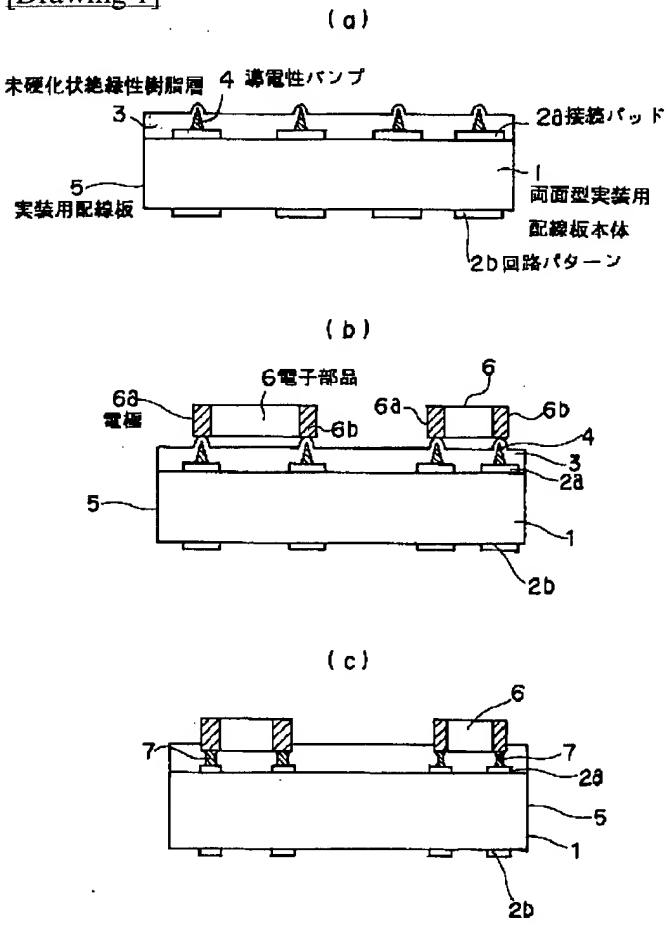
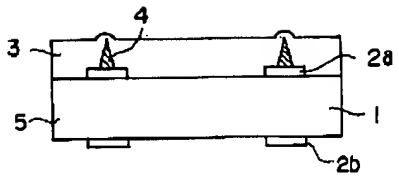
DRAWINGS

[Drawing 1]



[Drawing 2]

(a)



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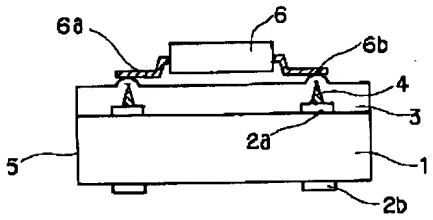
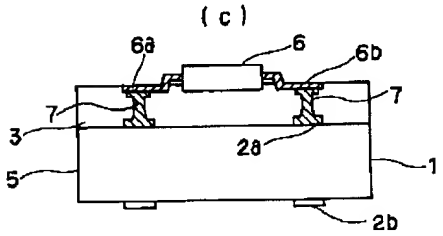
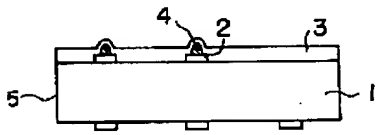


(c)



[Drawing 3]

(a)



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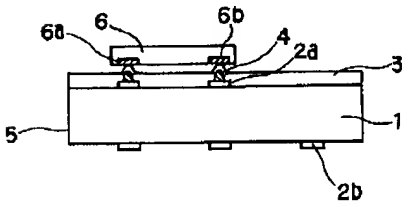
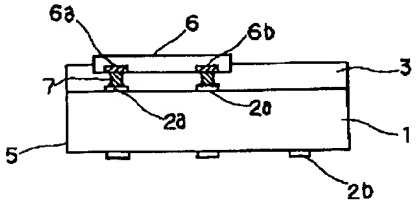


(c)



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